REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

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12-11-15

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TITLE

MICROCIRCUIT, LINEAR, DUAL CURRENT OUTPUT, PARALLEL INPUT, 16-BIT MULTIPLYING DAC WITH 4-QUADRANT RESISTOR, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/12651

REV

PAGE 1 **OF** 12

AMSC N/A

5962-V025-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual current output, parallel input, 16-bit multiplying DAC with 4-quadrant resistor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12651	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5547-EP	Dual current output, parallel input, 16-bit multiplying DAC with 4-quadrant resistor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	38	JEDEC MO-153-BD-1	Thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.3 V to +8.0 V
R_{FB}, R_{OFS}, R1, R_{COM} and VREF to GND	-18 V to +18 V
Logic inputs to GND	-0.3 V to +8 V
$V(I_{OUT})$ to GND	-0.3 V to V_{DD} + 0.3 V
Input current to any pin except supplies	±50 mA
Thermal resistance (θ_{JA}) 2/	
Maximum junction temperature ($T_{J\,MAX}$)	150°C
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Lead temperature:	
Vapor phase, 60 sec	215°C
Infrared, 15 sec	220°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Package power dissipation = $(T_{J\,MAX} - T_A)/\theta_{JA}$.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Address decoder pins. The truth table shall be as shown in figure 4.

3.5.5 Control inputs. The control inputs shall be as shown in figure 5.

3.5.6 Functional block diagram. The functional block diagram shall be as shown in figure 6.

3.5.7 16-bit 4-quadrant multiplying DAC with minimum of external components. The 16-bit 4-quadrant multiplying DAC with minimum of external components shall be as shown in figure 7.

3.5.8 Timing diagram. The timing diagram shall be as shown in figure 8.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Static performance 3/						
Resolution	N	1 LSB = $V_{REF}/2^{16}$ = 153 µV at V_{REF} = 10 V		16		Bits
Relative Accuracy	INL				±2	LSB
Differential nonlinearity	DNL	Monotonic			±1	LSB
Output leakage current	I_{OUT}	Data = zero scale, T_A = 25°C			10	nA
		Data = zero scale, T_A = T_A maximum			20	
Full scale Gain error	G_{FSE}	Data = full scale		±1	±5	mV
Bipolar mode Gain error	G_E	Data = full scale		±1	±5	
Bipolar mode Zero scale error	G_{ZSE}	Data = full scale		±1	±4	
Full scale temperature coefficient 4/	TCV_{FS}			1		ppm/°C
Reference input						
V_{REF} range	V_{REF}		-18		+18	V
REF input resistance	REF		4	5	6	kΩ
R1 and R2 resistance	R1 and R2		4	5	6	
R1 to R2 mismatch	Δ(R1 to R2)			±0.5	±1.5	Ω
Feedback and offset resistance	R_{FB}, R_{OFS}		8	10	12	kΩ
Input capacitance 4/	C_{REF}			5		pF
Analog output						
Output current	I_{OUT}	Data = full scale		2		mA
Output capacitance 4/	C_{OUT}	Code dependent		200		pF
Logic input and output						
Logic input low voltage	V_{IL}	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
Logic input high voltage	V_{IH}	V_{DD} = 5 V	2.4			
		V_{DD} = 3 V	2.1			
Input leakage current	I_{IL}				10	µA
Input capacitance 4/	C_{IL}				10	pF
Interface timing 4/ 5/ See FIGURE 8						
Data to $\overline{WR}$ setup time	t_{DS}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			
Data to $\overline{WR}$ hold time	t_{DS}	V_{DD} = 5 V	0			
		V_{DD} = 3 V	0			
$\overline{WR}$ pulse width	$t_{\overline{WR}}$	V_{DD} = 5 V	20			
		V_{DD} = 3 V	35			
LDAC pulse width	t_{LDAC}	V_{DD} = 5 V	20			
		V_{DD} = 3 V	35			
$\overline{RS}$ pulse width	t_{RS}	V_{DD} = 5 V	20			
		V_{DD} = 3 V	35			
$\overline{WR}$ to LDAC delay time	t_{LWD}	V_{DD} = 5 V	0			
		V_{DD} = 3 V	0			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Supply characteristics						
Power supply range	$V_{DD\ RANGE}$		2.7		5.5	V
Power supply current	I_{DD}	Logic inputs = 0 V			10	µA
Power dissipation	P_{DISS}	Logic inputs = 0 V			0.055	mW
Power supply sensitivity	P_{SS}	ΔV_{DD} = ±5%			0.003	%/%
AC characteristics 6/						
Output voltage settling time	ts	7/		0.5		µs
Reference multiplying bandwidth	BW	V_{REF} = 100 mV rms, data = full scale		6.8		MHz
Data glitch impulse	Q	V_{REF} = 0 V, midscale -1 to midscale		-3.5		nV-s
Multiplying feedthrough error	V_{OUT}/V_{REF}	V_{REF} = 100 mV rms, f = 10 kHz		-78		dB
Digital feedthrough	Q_D	$\overline{WR}$ = 1, LDAC toggles at 1 MHz		7		nV-s
Total harmonic distortion	THD	V_{REF} = 5 V p-p, data = full scale, f = 1 kHz		-104		dB
Output Noise density	e_N	f = 1 kHz, BW = 1 Hz		12		nV/√Hz
Analog crosstalk	C_{AT}	8/		-95		dB

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 2.7 V to 5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = -10 V to +10 V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.

3/ All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP97 I-to V converter amplifier. The device R_{FB} terminal is tied to the amplifier output. The +IN pin of the OP97 is grounded, and the I_{OUT} of the DAC is tied to the OP97's –IN pin. Typical values represent average readings measured at 25°C.

4/ Guaranteed by design, not subject to production test.

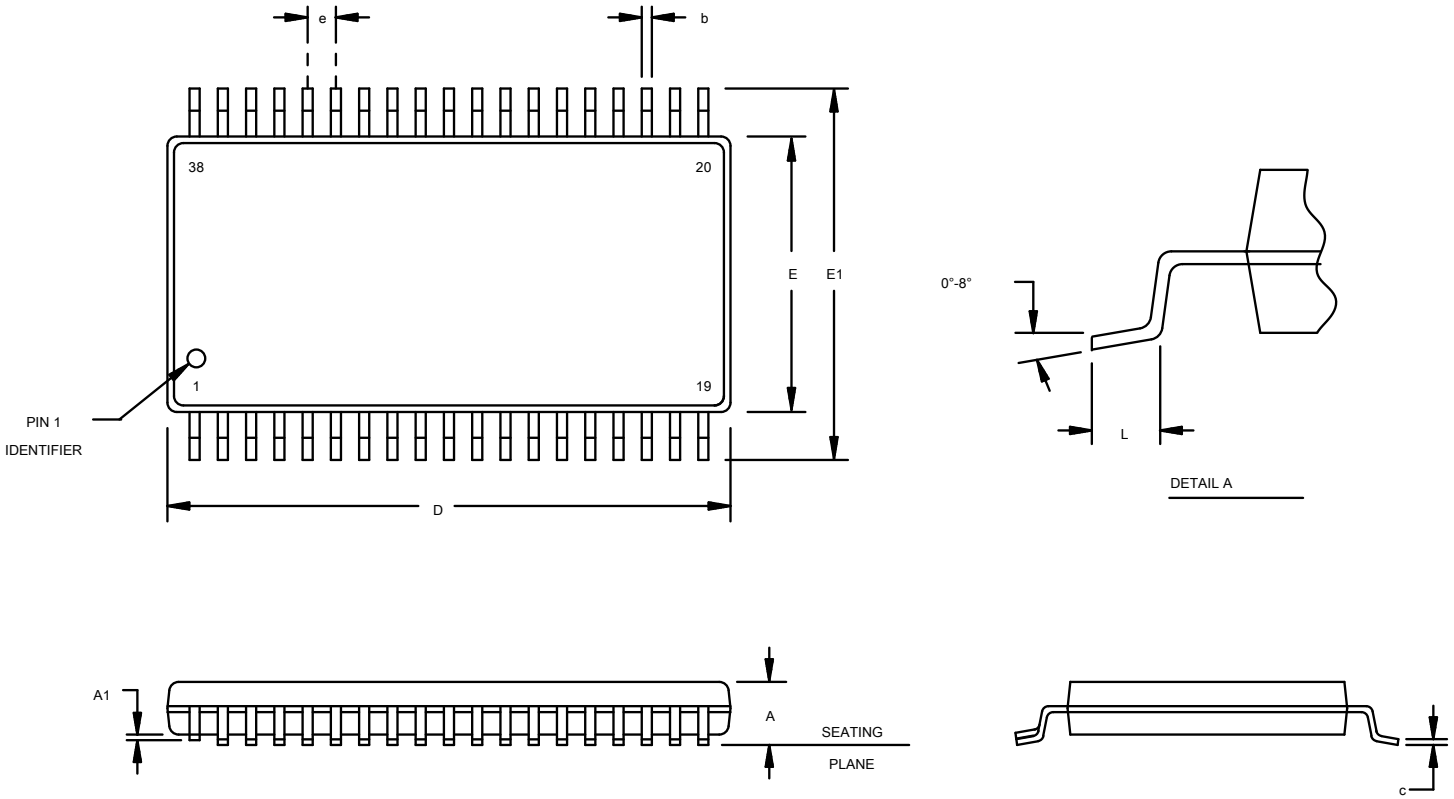
5/ All input control signals are specified with $t_r = t_f$ = 2.5 ns (10% to 90% of 3 V) and are timed from a voltage level of 1.5 V.

6/ All ac characteristic test are performed in a closed loop system using an AD8038 I-to-V converter amplifier except for THD where the AD8065 was used.

7/ To ±0.1% of full scale, data cycles from zero scale to full scale to zero scale.

8/ Signal input at channel A and measures the output at channel B, f = 1 kHz.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.17	0.27	e	0.50 BSC	
c	0.09	0.20	L	0.45	0.70
D	9.60	9.80			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-15-AB3.

FIGURE 1. Case outline.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D1	38	D2
2	D0	37	D3
3	R_{OFSA}	36	D4
4	R_{FBA}	35	D5
5	R_{1A}	34	D6
6	R_{COMA}	33	D7
7	V_{REFA}	32	D8
8	I_{OUTA}	31	D9
9	AGNDA	30	D10
10	DGND	29	VDD
11	AGNDA	28	D11
12	I_{OUTB}	27	D12
13	V_{REFB}	26	D13
14	R_{COMB}	25	D14
15	R_{1B}	24	D15
16	R_{FBB}	23	$\overline{RS}$
17	R_{OFSB}	22	MSB
18	$\overline{WR}$	21	LDAC
19	A0	20	A1

FIGURE 2. Terminal connections.

Terminal		Description
Number	Mnemonic	
1, 2.24 to 28, 30 to 38	D0 to D15	Digital input data bits D0 to D15. Signal level must be ≤ V_{DD} +0.3 V
3	R_{OFSA}	Bipolar offset resistor A. Accepts up to ±18 V. In 2-qudarant mode, R_{OFSA} ties to R_{FBA}. In 4-qudarant mode, R_{OFSA} ties to R_{1A} and the external reference.
4	R_{FBA}	Internal matching feedback resistor A. Connects to the external op amp for I-to-V conversion.
5	R_{1A}	4-Quadrant resistor. In 2-quadrant mode, R_{1A} shorts to the V_{REFA} pin. In 4-quadrant mode, R_{1A} ties to $R_{OFSA.}$. Do not connect when operating in unipolar mode.
6	R_{COMA}	Center tap point of the two 4-quadrant resistor, R_{1A} and R_{2A}. In 4-quadrant mode, R_{COMA} ties to the inverting node of the reference amplifier. In 2-quadrant mode, R_{COMA} shorts to the associated V_{REFA} pin. Do not connect when operating in unipolar mode.
7	V_{REFA}	DAC A reference input in 2 Quadrant mode, R2 terminal in 4-quadrant mode. In 2-quadrant mode, V_{REFA} is the reference input with constant input resistance vs code. In 4-quadrant mode, V_{REFA} is driven by the external reference amplifier.
8	I_{OUTA}	DAC A current output. Connects to the inverting terminal of external precision I-to-V op amp for voltage output.
9	AGNDA	DAC A analog ground.
10	DGND	Digital ground.
11	AGNDA	DAC B analog ground.
12	I_{OUTB}	DAC B current output. Connects to the inverting terminal of external precision I-to-V op amp for voltage output.
13	V_{REFB}	DAC B reference input pin. Establishes DAC full scale voltage. Constant input resistance vs code. If configured with an external op amp for 4-quadrant multiplying, V_{REFB} becomes $-V_{REF}$.
14	R_{COMB}	Center tap point of the two 4-quadrant resistor, R_{1B} and R_{2B}. In 4-quadrant mode, R_{COMB} ties to the inverting node of the reference amplifier. In 2-quadrant mode, R_{COMB} shorts to the associated V_{REFB} pin. Do not connect when operating in unipolar mode.
15	R_{1B}	4-Quadrant resistor. In 2-quadrant mode, R_{1B} shorts to the V_{REFB} pin. In 4-quadrant mode, R_{1B} ties to R_{OFSAB}. Do not connect when operating in unipolar mode.
16	R_{FBB}	Internal matching feedback resistor B. Connects to the external op amp for I-to-V conversion.
17	R_{OFSB}	Bipolar offset resistor B. Accepts up to ±18 V. In 2-qudarant mode, R_{OFSB} ties to R_{FBB}. In 4-qudarant mode, R_{OFSB} ties to R_{1B} and the external reference.
18	$\overline{WR}$	Write control digital input In, Active low. $\overline{WR}$ transfer shift register data to the DAC register on the rising edge. Signal level must be ≤ V_{DD} + 0.3 V.
19	A0	Address pin 0. Signal level must be ≤ V_{DD} + 0.3 V.
20	A1	Address pin 1. Signal level must be ≤ V_{DD} + 0.3 V.
21	LDAC	Digital input load DAC control. Signal level must be ≤ V_{DD} + 0.3 V.
22	MSB	Power-On Reset State. MSB = 0 corresponds to zero scale reset; MSB = 1 corresponds to midscale reset. The signal level must be ≤ V_{DD} + 0.3 V.
23	$\overline{RS}$	Active low resets both input and DAC registers. Reset to zero scale if MSB = 0 and reset to midscale if MSB = 1. Signal level must be ≤ V_{DD} + 0.3 V.
29	V_{DD}	Positive power supply input. The specified range of operation is 2.7 V to 5.5 V.

FIGURE 3. Terminal function.

A1	A0	Output update
0	0	DAC A
0	1	None
1	0	DAC A and DAC B
1	1	DAC B

FIGURE 4. Address decoder pins.

$\overline{RS}$	$\overline{WR}$	LDAC	Register Operation
0	X	X	Reset the output to 0 with MSB = 0; reset the output to midscale with MSB = 1
1	0	0	Load the input register with data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC registers are transparent.
1	⎍	⎍	When LDAC and $\overline{WR}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse and are then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation

FIGURE 5. Control Inputs

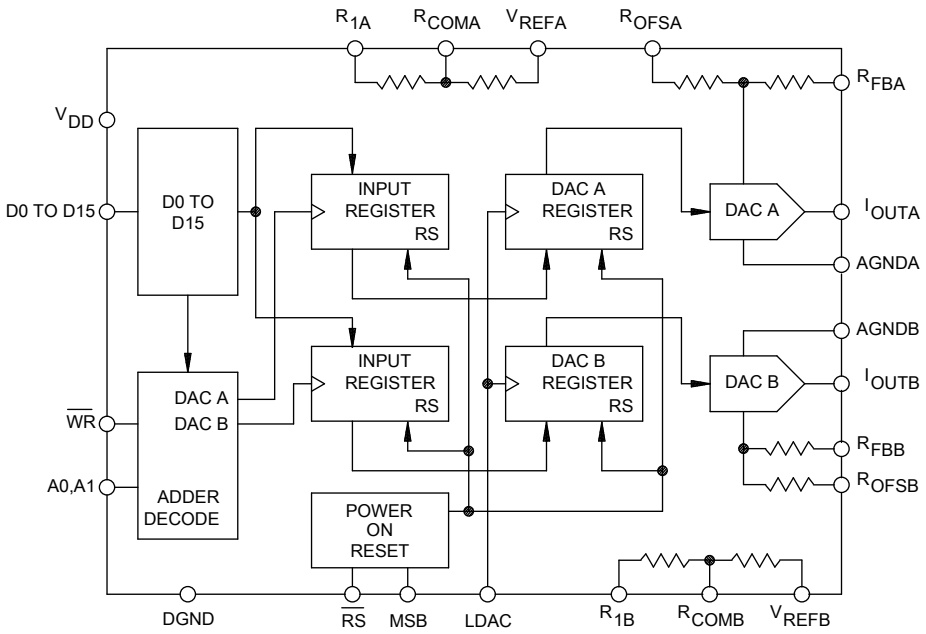


FIGURE 6. Functional block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12651
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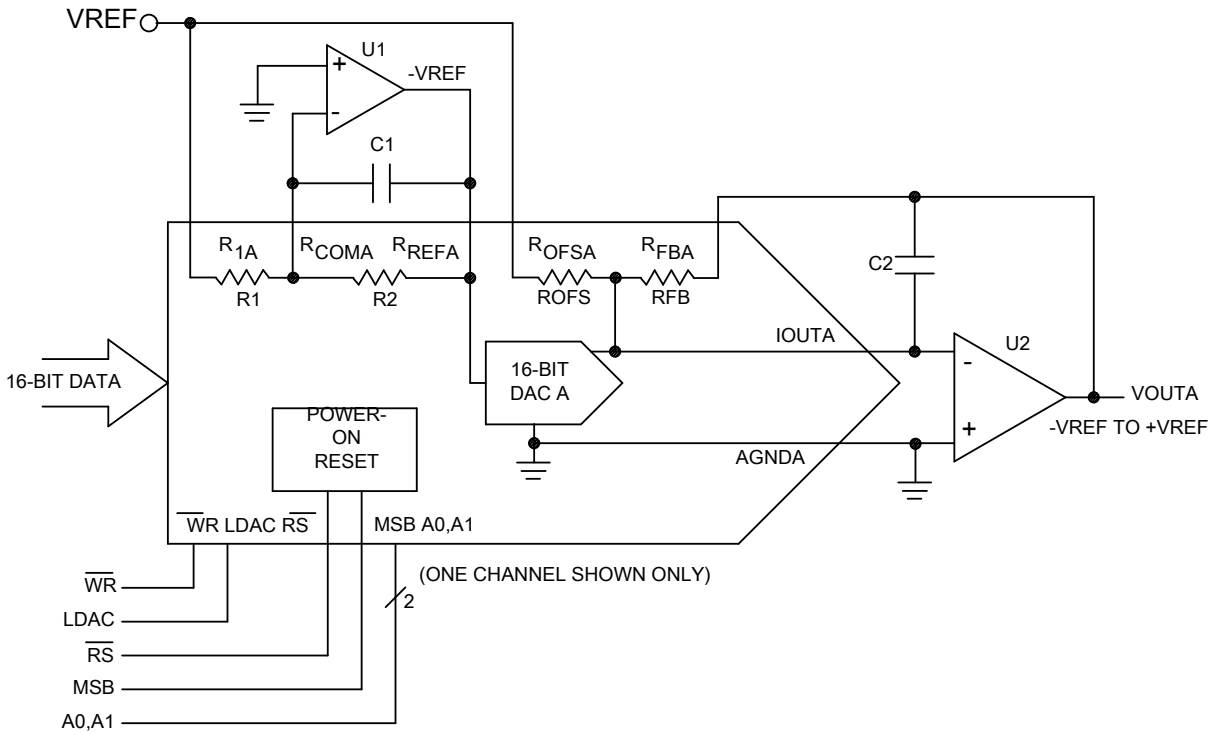

FIGURE 7. 16-bit 4-quadrant multiplying DAC with minimum of external components.

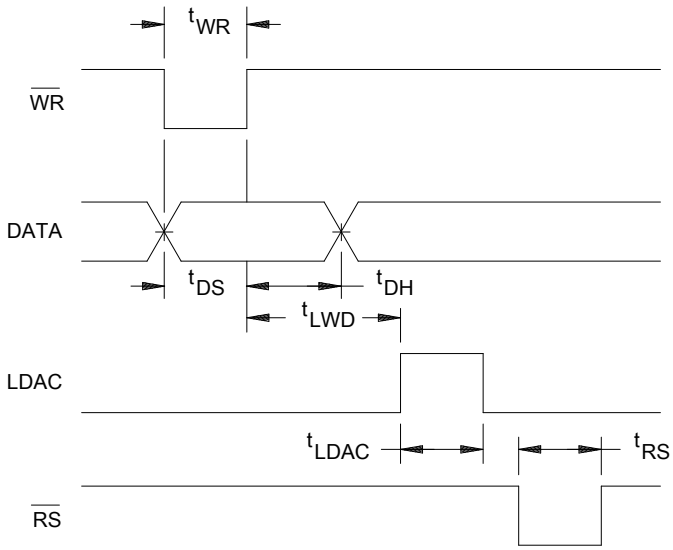

FIGURE 8. Timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12651-01XB	24355	AD5547SRU-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106